STORAGE DEVICE FOR A MULTIBUS ARCHITECTURE

~~Storage Device for a Multibus Architecture~~

BACKGROUND OF THE INVENTION

The invention relates in general to a multiple bus architecture associated with a signal processor and in particular to a memory storage device for use with such a multibus architecture ~~having the features listed in the preamble of Claim 1, a storage system having a plurality of storage devices, and a method for controlling such a storage device~~.

~~In order t~~To achieve a relatively high throughput of data in signal processors, these processors often include multiple connected read/write buses through which a single ~~one~~ data memory storage device may be accessed simultaneously. Control of memory addresses is typically implemented ~~here~~ through read/write buses by alternately transmitting addresses ~~data~~ and ~~information~~ data, or by transmitting addresses through a separate address bus apart from a data bus.

Where ~~In the case of~~ these systems involve~~ing~~ one or multiple data memories and ~~in~~ multiple buses~~,~~ ~~that is,~~ (i.e., a multibus architecture)~~,~~ the actual memory/bus connection is usually achieved in a manner which is relatively disadvantageous. ~~Currently, t~~Two approaches are commonly utilized to achieve relatively efficient memory access to store data in the memory~~,~~ or to read data from the memory. Either a multi-port memory is used which has multiple memory connections to access different buses, or the various buses are connected ~~only~~ to mutually independent memory blocks.

The first approach has the disadvantage that a multi-port memory is more complex and expensive to implement than a single-port memory. The second approach has the disadvantage that ~~the~~ separation of the memory blocks negatively affects program flexibility and execution

speed. For example, the memory partitioning must be defined within the program code, —a capability which is often not provided in high-level languages such as C.

What is needed is ~~The goal of the invention is therefore to propose~~ a memory storage device for a multibus architecture which enables more efficient memory access. ~~An additional goal is to propose a storage system having a plurality of such storage devices, as well as a method for operating such storage devices.~~

SUMMARY OF THE INVENTION

~~This goal is achieved by a storage device for a multibus architecture having the features of Claim 1, a storage system having a plurality of storage devices with the features of Claim 9, and a method for controlling such a storage device having the features of Claim 12.~~

~~The starting point of the invention is a~~A storage device for a multibus architecture includes ~~which comprises~~ at least one memory to store data, information, and/or addresses, along with ~~and~~ a memory connection having ~~with~~ a port to connect the memory to ~~a first~~one of the buses of the ~~a~~ multibus architecture,~~;~~ ~~wherein t~~The memory connection, the port, and the ~~first~~ bus have data lines to transmit data ~~and~~along with ~~, as required,~~ address lines to transmit addresses, and/or control information to control the memory and ~~, as required,~~ other devices connected to each ~~the~~ specific bus within the multibus architecture.

~~———~~A switching device ~~serves to~~ selectively connects the memory connection to one of the ~~first~~ buses ~~or an additional bus~~ to enable a memory access to transmit data, addresses, and/or control information to or from the selected one of ~~or to~~ these buses.

A storage system, specifically a storage system within a processor or separate from and ~~directly~~ connected to a processor, may have ~~advantageously has~~ a plurality of the ~~such~~ storage

devices ~~which are~~ selectively connected, ~~according to the method,~~ to ~~one~~ each one of the different buses.

~~Advantageous embodiments are the subject of the dependent claims.~~

~~The~~ The storage device may have ~~advantageously has~~ a memory-specific logic device and an interrupt line to transmit an interrupt signal to the processor, ~~which~~ The processor may controls operation of the ~~entire~~ storage system, ~~whereby t~~Transmission of the interrupt signal may triggers an interruption of the operation of the processor for, for example, one clock cycle whenever a memory access by the memory to the memory or memories of two different buses within two successive clock cycles is to be effected.

The memory may have ~~advantageously has~~ an address analyzer to analyze the addresses on the buses and/or the address lines assigned to the memory for memory accesses, and for ~~the purpose of~~ switching the switching device to one of the corresponding buses.

~~The~~ The analyzer ~~serves to~~ analyzes address segments and ~~to~~ switches and assigns memory access for address segments smaller than the word width of a bus or of address lines transmitting the addresses, such that the memory may be smaller than the actual required memory space. Additional data for storage may be ~~are~~ stored in a different memory.

An adjustable separator device, ~~specifically~~ (e.g., a programmably adjustable separator device), for storing the memory address or access address for the memory for analysis by the analyzer, allows the memory to assign any addresses ~~in order~~, for example, to be able to overlay external memories.

The analyzer may have ~~advantageously has~~ a common access control device to switch the switching device, and one comparator each per bus to compare the address with the memory address of the memory, thereby allowing the component-related expense to be reduced.

———The analyzer may ~~advantageously has~~ includes a modifier that ~~designed to~~ processes different data and/or access types which are applied —through data lines, subaddress lines, and/or access signal lines selected by the switching device —to a data memory segment of the memory ~~in order~~ to transmit the states on the bus lines.

A logic device to output a block loss signal through a loss line to the processor serves to issue a signal in response to a deviation from announced and executed data transfers during the memory access.

A ~~preferred~~ storage system may have ~~has~~ a plurality of such memories which are connected to a multibus architecture having a plurality of buses. ~~It is possible here to have a~~All or some of the memories may be ~~or only some of the memories~~ connectable ~~only~~ to some of the buses.

Specifically, during switching between read access and write access for one of the memories, different memories may be ~~are~~ controlled alternately by the clock cycle in a common process.

The use of such memories is advantageous particularly in the form of memories for a processor.

An interrupt signal to suspend the processor clock of a higher-level processor or to select a different memory may be ~~is advantageously~~ generated and issued whenever a memory access by the memory to two different buses, or by two different buses to the memory, is to be effected within two successive clock cycles ~~in order~~ to prevent loss of data.

———Having the processor use the logic device to generate a command such as a clock control signal to interrupt the processor clock or ~~such as~~ a memory select signal to select a different

storage device, and send this signal to the processor, prevents loss of data or drop-out periods during switching operations between read states and write states.

For memory accesses, address lines on the buses assigned to the memory, or address lines for determining the switching position of the switching device, may be ~~are~~ analyzed.

It is also possible ~~here~~ to search address segments smaller than the word width of the address as the assigned memory address during the analysis and to use the segments ~~them~~ as the switching criterion.— ~~t~~This is ~~being~~ advantageous for the distribution of data between multiple memories of this type.

———To this end, a method may be used in which the highest-value bit of the address to determine the access address is compared with an adjustable register, specifically a programmable register, and the memory access is enabled ~~only~~ in the case of a match.

———This procedure may be employed, for example, to implement an overlay procedure in which another memory, for example ~~specifically~~ a slower and larger memory is overlaid.

~~In order t~~To control a switching device, selected data lines, subaddress lines, and/or access signal lines of a selected bus are used to generate switching signals or commands in the event data or information transmitted over the selected bus does not match~~,~~ (in terms of the amount of data)~~,~~ the amount of memory space available per memory access operation.

~~The following discussion explains embodiments of the invention in more detail based on the drawings~~

These and other objects, features and advantages of the present invention will become more apparent in light of the following detailed description of preferred embodiments thereof, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.~~igure~~ 1 is a schematic block diagram illustration ~~view~~ of a storage device including a memory which may be connected to a multibus architecture using a switching device; and

FIG.~~igure~~ 2 is ~~shows~~ a schematic block diagram illustration of the ~~preferred~~ storage device of FIG. 1 including ~~a detailed illustration of~~ individual ~~preferred~~ components of a logic device to control the switching device.

DETAILED DESCRIPTION OF THE INVENTION

Referring to ~~Figure~~ FIG. 1, ~~shows how one embodiment of~~ a storage device 10 is connected to a multibus architecture 12, which may ~~here~~ includeing three buses 14-16~~P, D0, D1~~. The storage devices 10 includes ~~and functions shown and described here are only examples used to explain the basic principle of~~ a memory ~~M~~ 18 which may be selectively connected through a switching device 20 ~~SW~~ to one of the ~~multiple~~ buses 14-16~~P, D0, D1 of the multibus architecture~~. Any additional components that might be required to operate the ~~such a~~ storage device 10, such as address buses and other control buses, may be added in accordance with the commonly available technical knowledge.

The ~~A~~ memory 18 ~~M of this~~ is connected through the ~~type is in the form of and configured as memory M in a~~ multibus architecture 12 ~~of~~ to a processor 22 ~~PU~~ according to the preferred embodiment. The ~~P~~processor 22 may have ~~PU appropriately has~~ a storage system that includesing a plurality of the ~~such~~ memories 18~~M~~, of which one bus 14-16 each is able to be controlled simultaneously for a memory access. As used herein, ~~M~~memory access ~~here~~ means both the writing to the memory 18 ~~M~~ of data~~, specifically,~~ (e.g., information data), and the

reading of this data from a memory area of the memory 18 ~~M~~ through one of buses 14-16 ~~P, D0, D1~~. The ~~illustrated~~ buses 14-16 connect ~~P, D0, D1 lead directly~~ to the processor 22~~PU~~.; ~~although the relevant required~~ Other control devices, interface components, and the like are not shown in FIG. 1 since these components may be implemented in a ~~the conventional~~ manner that should be apparent to one of the ordinary skill in art. A pair of ~~The same applies to~~ control signals on lines 24, 26 ~~BML, STL which~~ transmit, for example, a block loss signal on the line 24~~bm~~, and ~~or~~ an interrupt signal on the line 26.~~st,~~ ~~or o~~Other commands may be transmitted on these lines 24, 26 to the processor 22.

The ~~actual memory or~~ memory area 18 ~~M~~ of the storage device 10 has a memory connection 28 ~~B~~ in the form of a memory port of the conventional type. The memory connection is connected to the switching device 20 ~~SW~~ through data lines 30 which may be part ~~DL or through the data lines DL~~ of a data bus. The ~~S~~switching device 20 ~~SW~~ selectively switches the data lines 30 ~~DL~~ through corresponding lines 32-34 ~~PL, D0L, D1L~~ and external ports 36-38 ~~BP, B0, B1~~ to one of the buses 14-16~~P, D0 or D1~~.

A ~~L~~logic device 40 ~~L serves to~~ switches the switching device 20~~SW~~, which ~~logic device~~ is connected preferably to additional devices such as a memory separator register or ~~(~~memory tag register 42 ~~) MTR~~ and at least one comparator 44~~CU~~. The block loss signal on the line 24 ~~BML here~~ starts, for example, from the comparator 44 ~~CU~~ and leads to the processor 22~~PU~~, while the interrupt signal line 26 ~~STL~~ leads from the ~~actual~~ logic device 40 ~~L~~ to the processor 22~~PU~~.

In a preferred embodiment, a conventional common data memory may be ~~is~~ subdivided into multiple blocks or storage devices functioning as the storage system of the processor ~~PU~~, which blocks, for example comprising the ~~like~~ memory 18~~M shown~~, may have ~~only~~ a single internal access connection 28~~B~~. The ~~M~~multiple read/write buses 14-16 ~~P, D0, D1~~ are connected

to each of these memories 18 ~~M~~ through the switching device 20~~SW~~. The logic device 40 integrated within the block or storage device 10 acts as an access control device and controls the memory access of the different buses 14-16 to the block 10 and to the memory 18 ~~M~~ located in the block, or of the memory 18 ~~M~~ to one of the buses 14-16 ~~P, D0, D1~~. It is not ~~absolutely~~ necessary ~~, of course,~~ that each of the memories 18 ~~M~~ be connectable to all of the buses 14-16 ~~P, D0, D1~~.

Whenever two of the buses 14-16 ~~P, D0, D1~~ are to simultaneously access the same memory 18, ~~M,~~ the logic device 40 ~~L~~ sends the interrupt signal on the line 26 ~~st through interrupt signal line STL~~ to the processor 22 ~~PU~~ or to a clock control device of the processor 22 ~~PU so as~~ to suspend the processor clock ~~for the processor~~ for one clock cycle.~~,~~ This ~~thereby~~ allows~~ing~~ the switching device 20 ~~SW~~ to switch successive accesses to the two requesting buses 14-16 and the corresponding states to be transmitted on the bus lines 14-16. Alternatively, appropriate programming and/or an appropriate wiring layout of the processor 22 may ~~PU is able to~~ handle the suspension of the processor clock.

Specifically, write access is possible in smaller units than the word width of the buses 14-16 without losing a clock cycle~~;, that is,~~ for example, byte-by-byte accessing for a 32-bit bus. The actual read-modify-write operation for this example ~~here~~ requires the usual two clock cycles. ~~In order t~~To prevent the loss of a clock cycle, ~~either~~ buffering is implemented by the logic device 40 ~~L~~ on the incoming side of the memory 18 ~~M~~ and by any other devices connected to the~~is~~ logic device~~,~~ 40. In the alternative, ~~or~~ an appropriate access control signal on the line 26 may be ~~st is~~ exchanged with the processor 22 so ~~PU in order~~ that the~~is~~ memory 18 ~~M~~ may not be acted upon during the next clock cycle and ~~so that~~ the processor 22 ~~PU~~ does not need to be suspended, but instead accesses a different memory 18 ~~M~~ during this next clock cycle.

The memory-block-specific logic device 40 may be ~~L is advantageously~~ expanded~~able~~ by using the ~~a~~ comparator 44 ~~CU~~ which compares the highest-value bit of the address with an adjustable register, for example, ~~specifically,~~ a register adjustable by programming, ~~and only~~ operates in the event ~~case~~ of a match.; ~~with t~~The result is that the individual memories 18 ~~M~~ of a plurality of such memories 18 ~~M~~ are able to be arranged in any manner ~~fashion~~ within a linear address space. For example, a memory of a slow external memory module may be overlaid by a memory access to the memory 18~~M~~, then copied back upon termination of a corresponding dedicated program segment. This method, ~~in fact well~~ known as the overlay procedure, enables fast access to the data despite the fact that the internal memory ~~M~~ of the processor may be smaller than the memory required for the application. A relatively larger required memory area is thus appropriately managed by splitting among multiple smaller memories 18~~M~~.

The ~~M~~memory 18 ~~M~~ in FIG.~~igure~~ 1 has only one data line or data bus 30~~DL~~. In principle, it is possible to transmit address data and information data in temporal sequence over a single bus, where the address data indicate to which, or from which, the memories 18 ~~M~~ or addresses within the memory 18 ~~M~~ the information data are to be transmitted as the actual data~~d~~. Alternatively, it is possible to employ a separate address bus through which exclusively address data are transmitted, with the result that only actual useful data, and possibly additional address or control information, are transmitted through the data bus 30~~DL~~.

Referring to ~~Figure~~ FIG. 2, ~~illustrates a detailed embodiment, in which again~~ a memory 100 ~~M having preferably~~ having a plurality of addressable memory locations is connectable through switching device 102 ~~SW~~ to one of multiple buses 104-107 ~~P, D0, D1, R~~ of a multibus architecture 110.

~~In the example shown, memory c~~Connections to the memory 100 include ~~B is subdivided into~~ an address memory connection 114 and a data memory connection 116. The addresses for addressing internal memory locations of the memory 100~~M~~, which may be ~~are~~ transmitted through a separate address bus or ~~, as described above,~~ through one of the buses 104-107, ~~P, D0, D1, R,~~ are applied to the address memory connection 114. ~~In the embodiment shown, in each case t~~The address information is supplied from the actively switched bus 104~~P~~.

~~———~~It is also possible ~~specifically here also~~ to have addresses supplied ~~only~~ through the ~~a~~ bus 104 ~~P~~ in the form of a programming bus such that the switching device 102 ~~SW~~ implements switching to the programming bus 104 ~~P~~ routinely or upon completion of a memory access. To implement a data access, the switch-over to the required additional bus 105-107 ~~D0, D1, R~~ is effected as required.

Starting from the buses 104-107 ~~P, D0, D1, R,~~ which may, for example, be 32-bit buses, a 32-bit line 118 leads to a data input switch of the switching device 102~~SW~~. Depending on the switching position of the switching device 102~~SW~~, a 32-bit data line or a 32-bit data bus 118 ~~DL~~ is thus routed from the selected bus 104-107 ~~P, D0, D1, R~~ through the switching device 102 ~~SW~~ to the data memory connection 116. ~~of data connection B in order~~ This is done to write or read the relevant data or line states to or from the memory area of the memory 100 being ~~M~~ addressed ~~at this moment~~.

The d~~D~~ata line 118 ~~DL~~ which leads from each bus 104-107 ~~P, D0, D1, R~~ to the corresponding switching connection of the switching device 102 ~~SW~~ has a splitter 120 ~~SP~~ at the input of a logic device 122 ~~L~~ composed of a plurality of individual components. ~~,~~ The ~~which~~ splitter 120 may~~is~~, for example, be in the form of a tap, where~~in~~ the individual data lines of the data bus 118 ~~DL~~ are tapped and routed as address lines 124 ~~AL~~ to a divider 126 ~~DIV~~. In this

example, the divider 126 ~~DIV~~ separates out ten address lines 125 ~~AL~~ and routes these lines 125 to an appropriately connected address line input of the switching device 102~~SW~~. Depending on the switching position, the address signal of the selected bus 104-107 ~~P, D0, D1, R~~ is thus applied to the address memory input of ~~address~~ connection 114 ~~B~~ of the memory 100~~M~~.

In addition, two address lines 128 ~~SAL~~ are separated out from each divider 126 ~~DIV~~ to transmit subaddresses, then routed to an appropriately connected input of the switching device 102 ~~SW~~ which passes on the subaddress of the selected bus 104-107 ~~P, D0, D1, R~~ to a modifier 130~~MOD~~.

Each ~~The~~ splitter 120 ~~SP~~ also splits the data lines 118 (e.g., ~~for example,~~ four ~~of~~ lines 132 ~~ACL~~ with information about the access type) ~~—~~from the ~~actual~~ data lines 118 ~~32~~ and routes these four lines 132 to an appropriately connected input of the switching device 102~~SW~~. The~~is~~ switching device 102 also applies the signals or states of ~~address~~ access type lines 132 ~~ACL~~ to the modifier 130 ~~MOD~~ depending on the switching position of the selected bus 104-107~~P, D0, D1, R~~.

The ~~M~~modifier 130 may ~~MOD is~~ also be interconnected between the switched data line 118 ~~DL~~ and the data memory connection ~~B~~. The ~~M~~modifier 130 ~~MOD~~ serves to modify the received data ~~d~~ from the selected bus 104-107 ~~P, D0, D1, R~~ and determines, in terms of the access type~~,~~ (e.g., ~~specifically~~ a write access or read access), whether what is found on the data line 118 ~~DL~~ is a complete word, shortened word ~~(short)~~, or ~~only~~ one byte from an original data word which is to be transmitted during the memory access, or if it is a label or signal that has been extended in some way.

In addition, the modifier 130~~MOD~~, among other functions, passes on a read-modifier-write signal on a line 134 to an access control device 136 ~~ARB~~ forming an additional component

of the logic device 122~~L~~. In connection with a processor 138~~PU~~, the access control device 136 ~~ARB~~ controls access to the memory 100~~M~~. The ~~A~~access control device 136 ~~ARB~~ additionally controls the operation of the switching device 102~~SW~~.

The ~~M~~memory logic 122~~L~~, as the analyzer or part of the analyzer, may also have ~~advantageously has~~ a memory separator register or memory tag register 140 ~~MTR~~ which is programmable, for example through the bus 107~~R~~, with the access address of the memory 100~~M~~. The ~~M~~memory tag register 140 may ~~MTR advantageously~~ also have an overflow signal on a line 142~~AGL to~~ provided to it by the processor 138 for memory overflow protection.

Twenty of the ~~A~~address lines 124 ~~AL, here 20 of the address lines,~~ branch off from each divider 126.~~DIV,~~ ~~e~~Each of these twenty address lines 144 ~~which~~ are routed to a comparator 146~~CU~~. Each ~~C~~comparator 146 ~~CU~~ compares the ~~thus~~ received address data with the address data stored in the memory tag register 140 ~~MTR~~ and provides the comparison result to the access control device 136 ~~ARB~~ for further processing.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is: